

LH532100B-1

CMOS 2M (256K × 8) Mask-Programmable ROM

FEATURES

- 262,144 words × 8 bit organization
- Access time: 120 ns (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Power consumption:
 - Operating: 275 mW (MAX.)
 - Standby: 550 μW (MAX.)
- Mask-programmable control pin:
 - Pin 1 = $OE_1/\overline{OE}_1/DC$
 - Pin 24 = OE/\overline{OE}
- Packages:
 - 32-pin, 600-mil DIP
 - 32-pin, 525-mil SOP
 - 32-pin, 450-mil QFJ (PLCC)
 - 32-pin, 8 × 20 mm² TSOP (Type I)
 - 32-pin, 400-mil TSOP (Type II)

DESCRIPTION

The LH532100B-1 is a CMOS 2M-bit mask-programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate process technology.

PIN CONNECTIONS

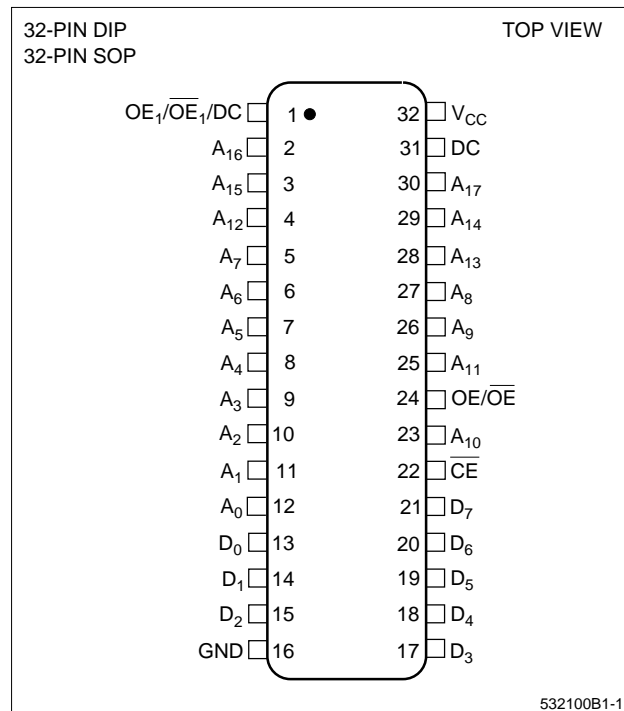


Figure 1. Pin Connections for DIP and SOP Packages

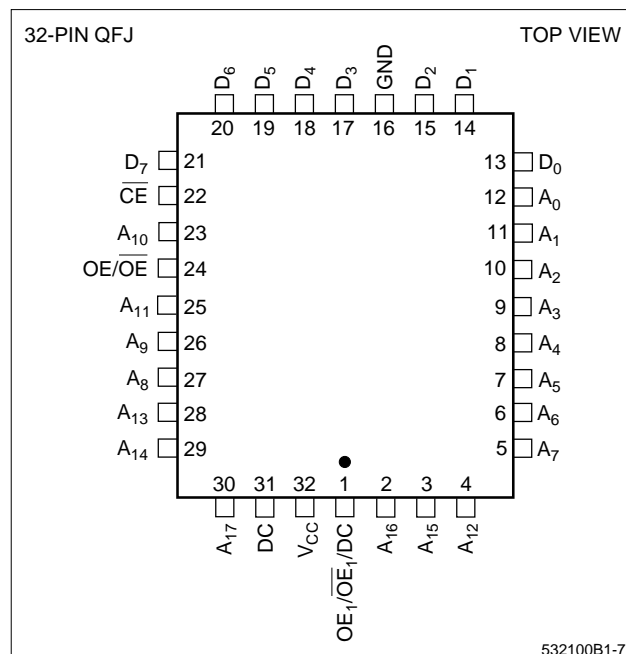


Figure 2. Pin Connections for QFJ (PLCC) Package

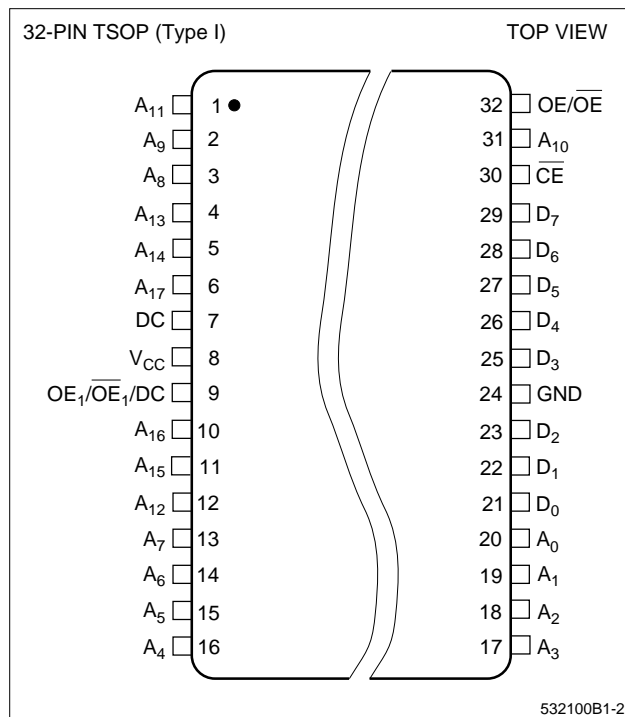


Figure 3. Pin Connections for TSOP (Type I) Package

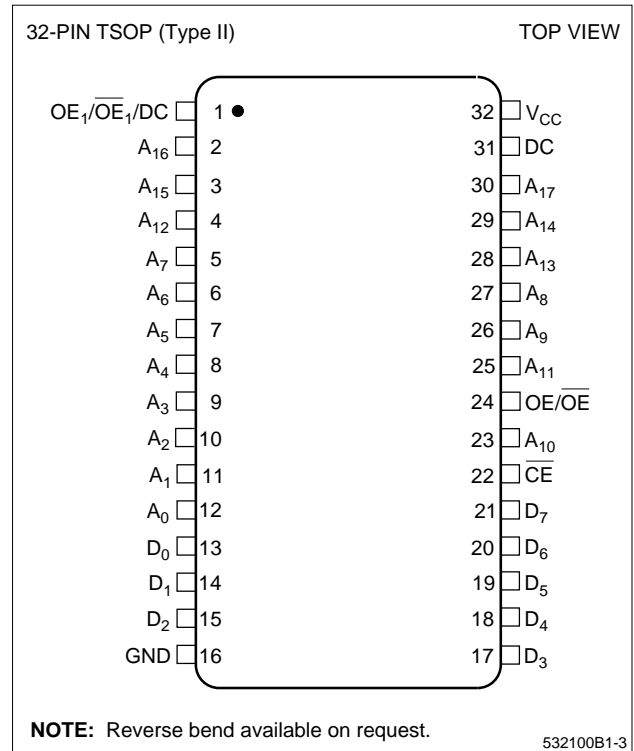


Figure 4. Pin Connections for TSOP (Type II) Package

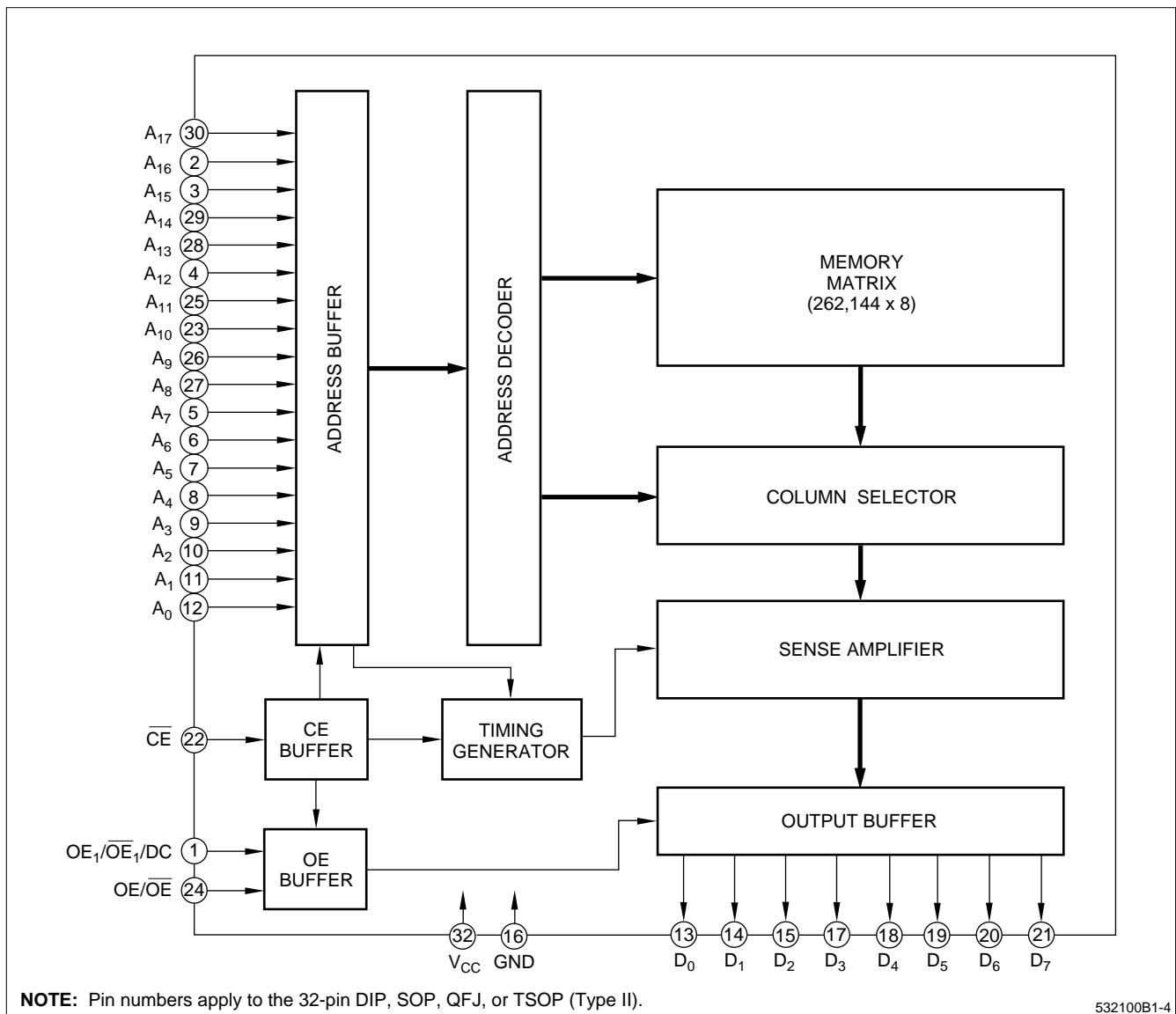


Figure 5. LH532100B-1 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₀ – A ₁₇	Address input	
D ₀ – D ₇	Data output	
\overline{CE}	Chip enable input	
OE/ \overline{OE}	Output enable input	1

SIGNAL	PIN NAME	NOTE
OE ₁ / \overline{OE} ₁ /DC	Output enable input	1, 2
V _{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

- Active levels of OE/ \overline{OE} and OE₁/ \overline{OE} ₁/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.
- DC = Don't care.

TRUTH TABLE

\overline{CE}	OE/ \overline{OE}	OE ₁ / \overline{OE} ₁	DATA OUTPUT	SUPPLY CURRENT
H	X	X	High-Z	Standby
L	L/H	X	High-Z	Operating
L	X	L/H	High-Z	Operating
L	H/L	H/L	Output	Operating

NOTE:

X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}		2.2	V _{CC} + 0.3	V	
Input 'Low' voltage	V _{IL}		-0.3	0.8	V	
Output 'High' voltage	V _{OH}	I _{OH} = -400 μA	2.4		V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA		0.4	V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 120 ns		50	mA	2
	I _{CC2}	t _{RC} = 1 μs		45	mA	2
	I _{CC3}	t _{RC} = 120 ns		45	mA	3
	I _{CC4}	t _{RC} = 1 μs		40	mA	3
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$		100	μA	
Input capacitance	C _{IN}	f = 1 MHz		10	pF	
Output capacitance	C _{OUT}	T _A = 25°C		10	pF	

NOTES:

1. $\overline{CE}/\overline{OE}/\overline{OE}_1 = V_{IH}$, OE/OE₁ = V_{IL}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE} = 0.2 V$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable access time	t_{ACE}		120	ns	
Output enable delay time	t_{OE}		50	ns	
Output hold time	t_{OH}	10		ns	
CE to output in High-Z	t_{CHZ}		50	ns	1
OE to output in High-Z	t_{OHZ}				

NOTE:

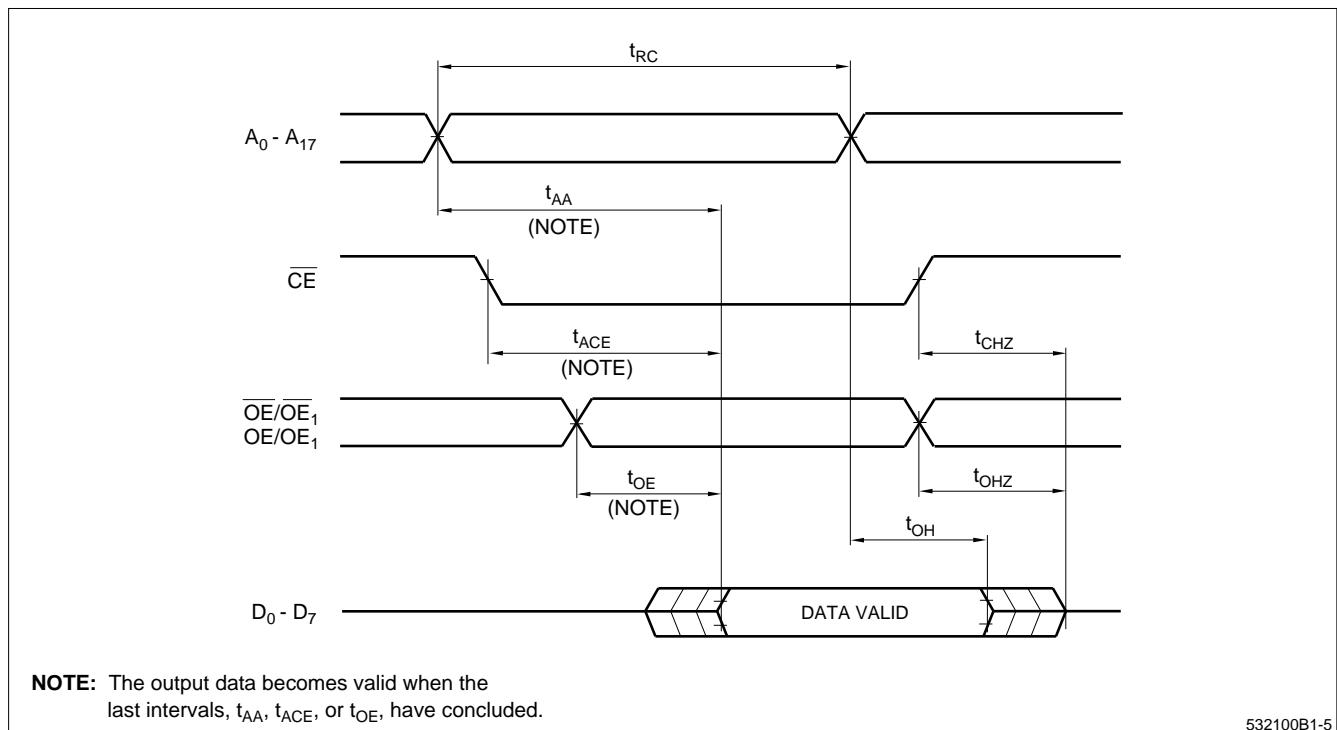
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1 TTL + 100 pF

CAUTION

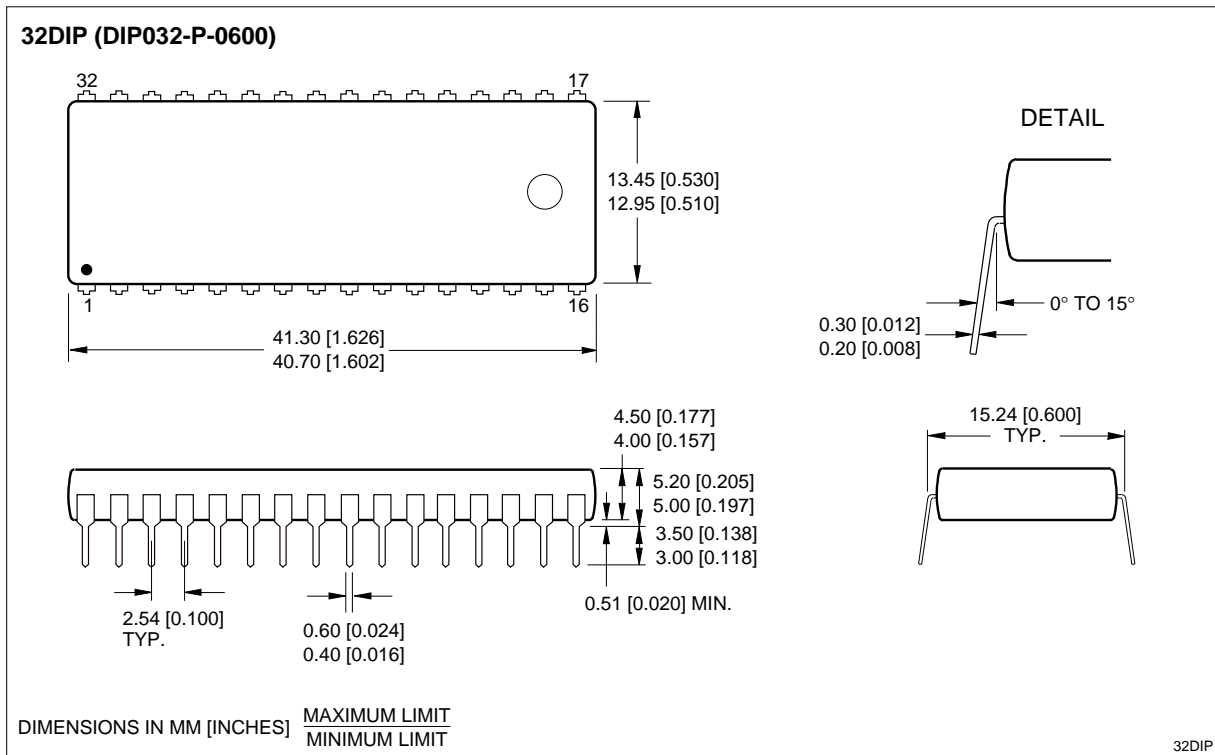
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



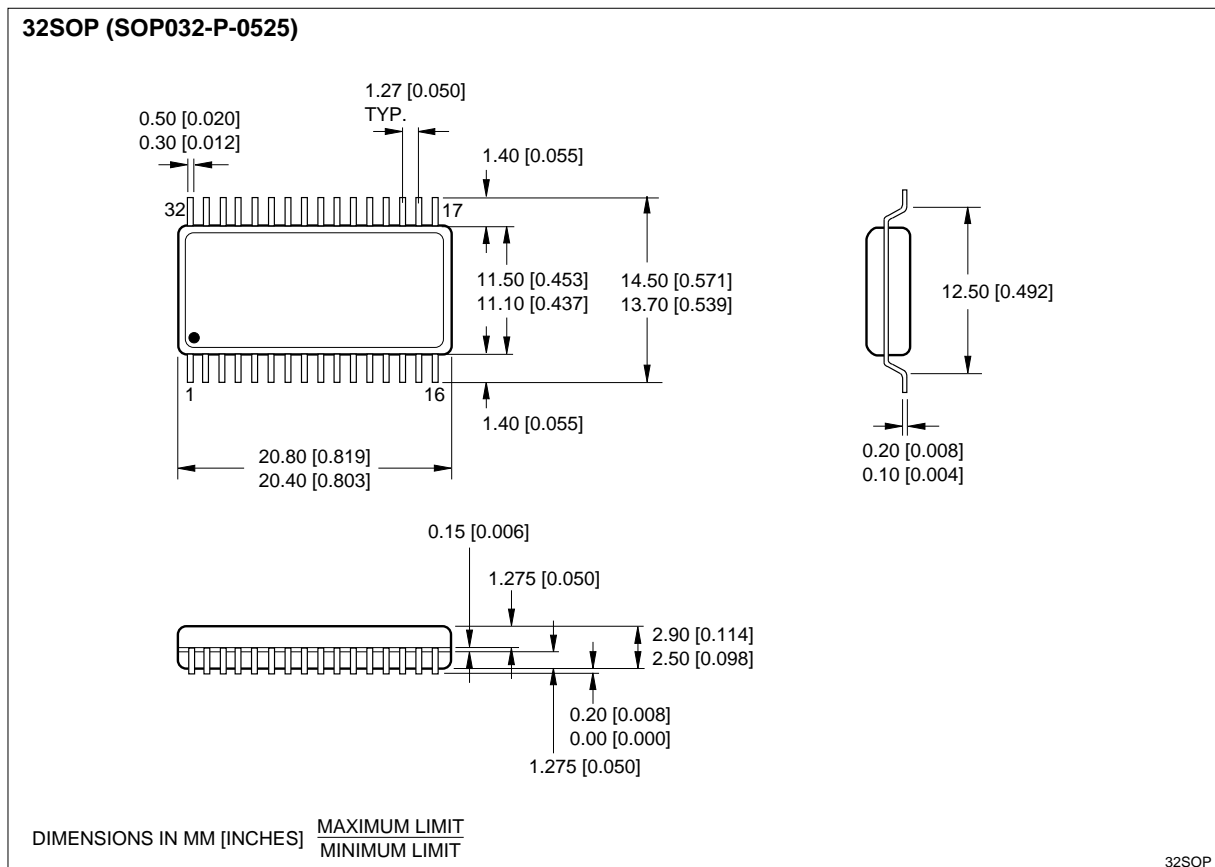
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Figure 6. Timing Diagram

PACKAGE DIAGRAMS

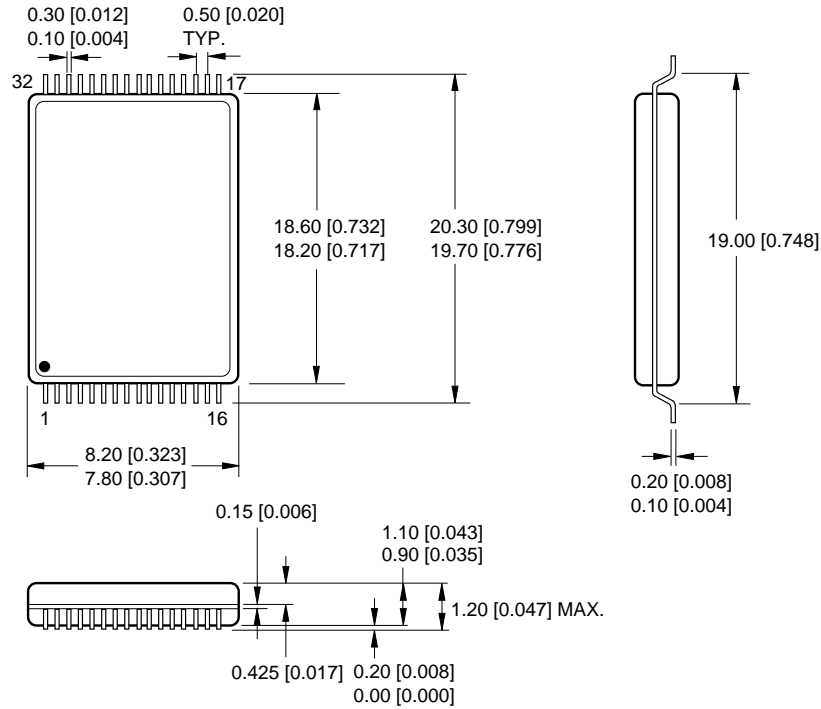


32-pin, 600-mil DIP



32-pin, 525-mil SOP

32TSOP (Type I) (TSOP032-P-0820)

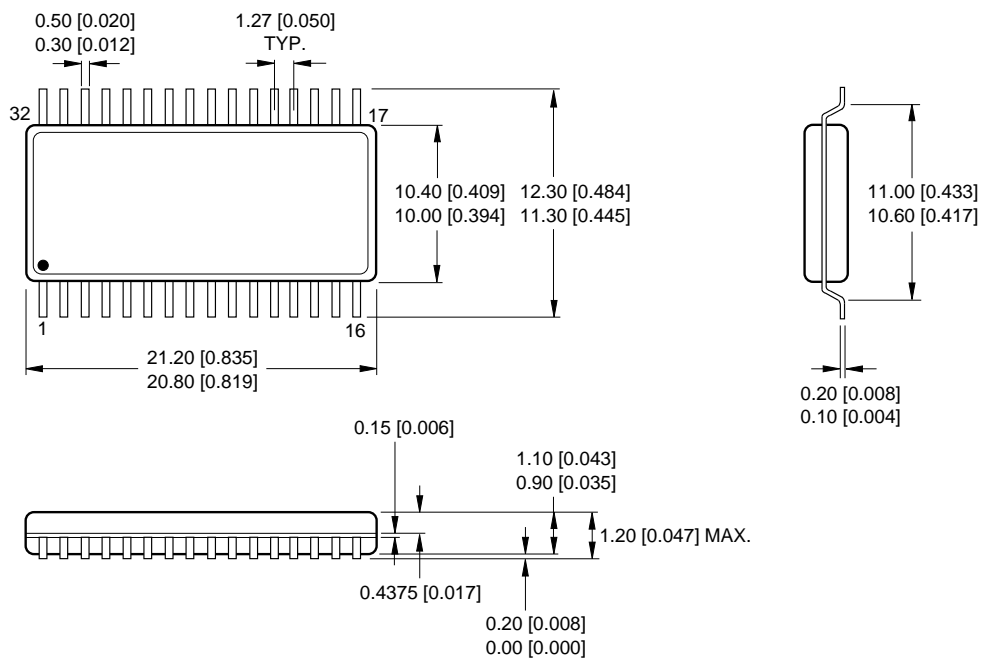


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

32TSOP

32-pin, 8 × 20 mm² TSOP (Type I)

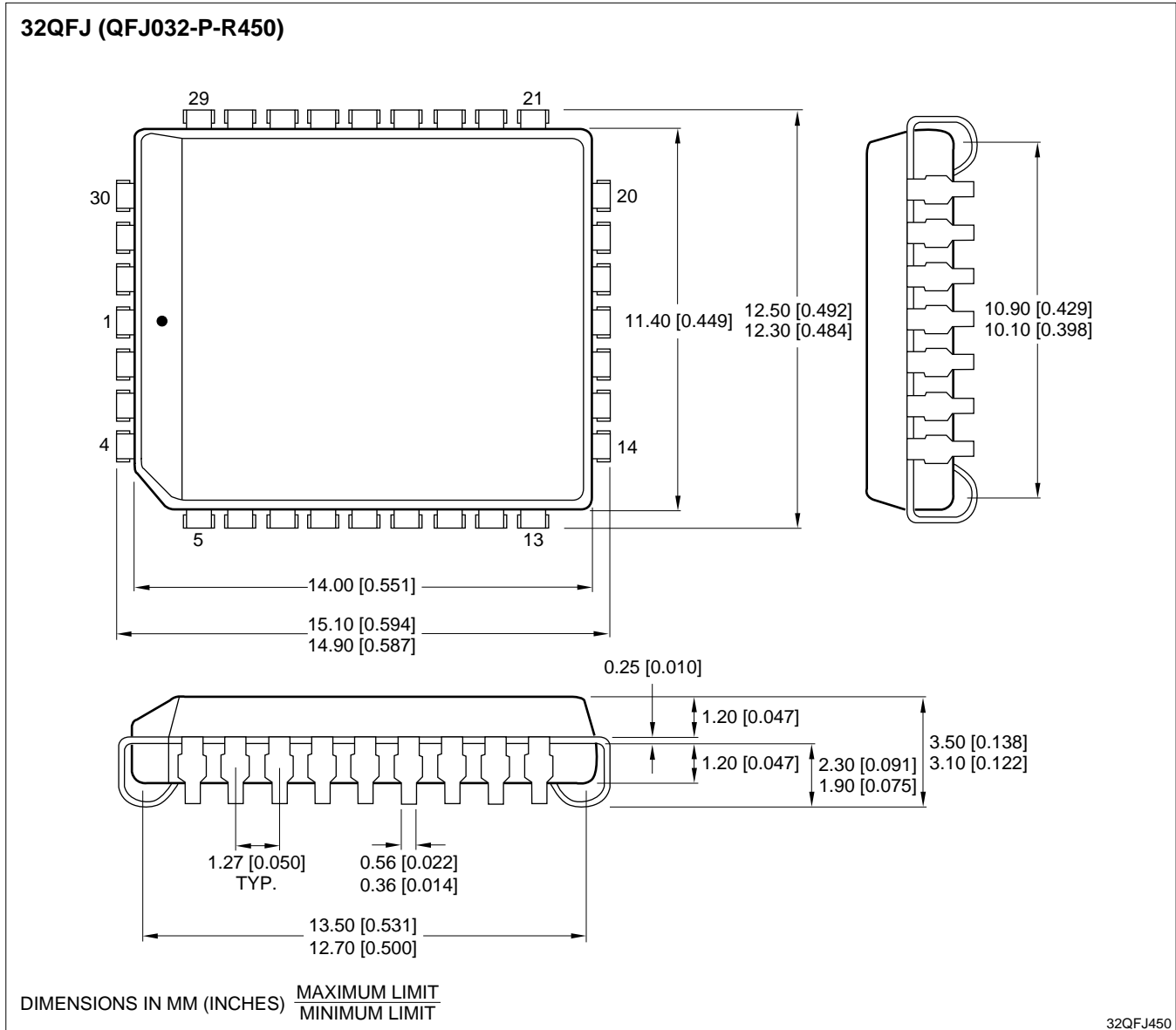
32TSOP (Type II) (TSOP032-P-0400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

32TSOP400

32-pin, 400-mil TSOP (Type II)



32-pin, 450-mil QFJ (PLCC)

ORDERING INFORMATION

LH532100B	X	-1	
Device Type	Package	120 ns Version	
			<ul style="list-style-type: none"> D 32-pin, 600-mil DIP (DIP032-P-0600) N 32-pin, 525-mil SOP (SOP032-P-0525) U 32-pin, 450-mil QFJ (PLCC) (QFJ032-P-R450) T 32-pin, 8 x 20 mm² TSOP (Type I) (TSOP032-P-0820) S 32-pin, 400-mil TSOP (Type II) (TSOP032-P-0400) SR 32-pin, 400-mil TSOP (Type II) Reverse bend (TSOP032-P-0400)
			CMOS 2M (256K x 16) Mask-Programmable ROM
Example: LH532100BD-1 (CMOS 2M (256K x 8) Mask-Programmable ROM, 32-pin, 600-mil DIP)			

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